**National University of Computer and Emerging Sciences**

**(Islamabad Campus)**

Department of Computer Science

**Signature of Invigilator: \_\_\_\_\_\_\_\_\_\_\_\_\_\_ Serial No:\_\_\_\_\_\_\_\_\_**

EE-105 Computer Logic Design

Mid-II Examination (Spring 2013)

**Instructor(s):**

Dr Ayub Alvi, Ms Mehreen Alam, Mr Adnan Saeed

Monday April 8,2013

**Total Marks: 40 Time Allowed: 1 hour**

Please read the instructions carefully:

1. Understanding the question paper is also part of the exam, so do not ask any clarification.
2. Solve questions in the space provided, or if you need more space write on the back side of the paper and clearly mark question and part number etc..
3. It is a CLOSED book/notes exam.
4. Calculators are NOT allowed.
5. Write your name and roll number on each page.
6. The question paper is printed on both sides of the pages.
7. Use permanent ink pens only. Any part done using soft pencil will not be marked and cannot be claimed for rechecking.

**Roll No: \_\_\_\_\_\_\_\_\_ Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Signature\_\_\_\_\_\_\_\_\_\_\_\_ Sec: \_\_\_**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Question | 1 | 2 | 3 | 4 | Total |
| Total Marks | 10 | 10 | 10 | 10 | 40 |
| Marks Obtained |  |  |  |  |  |

Vetted By: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Vetter Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**Question # 1[10 = 1, 1, 1, 1, 2, 2, 2]**

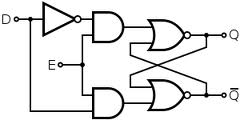
Table below converts the 4-bit (ABCD) Gray code to 4-bit (WXYZ) Binary code.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| A | B | C | D |  | W | X | Y | Z |
| 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 |  | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |  | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 |  | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 |  | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |  | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 |  | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 |  | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 |  | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 |  | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 |  | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 |  | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 |  | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 |  | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |  | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |  | 1 | 1 | 1 | 1 |

1. Write the output W in the form of min-terms
2. Write the output X in the form of max-terms
3. Write the output Y as function ∑ (………)
4. Write the output Y as function π (………)
5. Draw a k-map for output Z and write minimized expression in the form of SoP
6. Draw a k-map for output X and write minimized expression in the form of PoS
7. Draw the **simplified** combinational circuit for all the four outputs (W, X, Y, Z)

**Question # 2[10 = 5, 5]**

1. Implement a 4-to-16 decoder using 3-to-8 decoders only.
2. Draw the function table for the following D-latch.



|  |  |  |
| --- | --- | --- |
| Enable | D | Qt+1 |
|  |  |  |
|  |  |  |
|  |  |  |

**Question # 3[10 = 3, 3, 4]**

Implement the function F = ∑ (1, 5, 12, 14, 15) using the following three techniques using:

1. a 4-to-16 decoder only
2. a 16-to-1 MUX only
3. a 8-to-1 MUX only

**Question # 4[10 = 6, 2, 2]**

Minimize the function F = ∑ (0, 1, 3, 5, 6, 7) using Quine-McCluskey Method. Also list the

1. ‘Prime Implicants’ and
2. ‘Essential Prime Implicants’ of this function